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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/625,578	SMITH ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Amendment mailed on February 23, 2004. Claims 1-36 of the application are pending. This office action is made non-final.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and further in view of **Hanf et al.** (U.S. Patent 6,438,462).

4.1 **Chen et al.** teaches On-chip decoupling capacitor optimization for high-performance VLSI design. Specifically as per Claim 1, **Chen et al.** teaches a system for determining decoupling components for a power distribution system (Abstract, L1-4; Page 99, CL1, Para 3); the system comprising:

a database of characteristic values for a plurality of decoupling components (Page 99, CL1, Para 3; Page 99, CL2, Para 1); and

a computer system configured to:

access the database of characteristic values for the plurality of decoupling components (Page 99, CL1, Para 3; Page 99, CL2, Para 1);

accept known system parameters for the power distribution system (Page 99, CL1, Para 3; Page 100, CL1, Para 1);

select one or more different decoupling components based on the known system parameters for the power distribution system and entries in the database (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 100, CL1, Para 1);

calculate a specific quantity for selected decoupling components, the selected decoupling components selected from the database based on known system parameters (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 4); and

determine a location of placement within the power distribution system for each of the selected decoupling components based on the known system parameters and the entries in the database (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 3).

Chen et al. does not expressly teach the power distribution system including a voltage regulator module. **Peil** teaches the power distribution system including a voltage regulator module (Fig 2; CL7, L11-30; CL8, L4-13; CL8, L65-68; CL9, L33-40, L61-65; CL12, L33 to CL13, L15; CL13, L32-48; Fig 6), as the voltage regulation stabilizes the output voltage to within allowable tolerance (CL8, L10-12; CL12, L59-64). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included the power distribution system including a voltage regulator module, as the voltage regulation would stabilize the output voltage to within allowable tolerance.

Chen et al. does not expressly teach simulating a voltage regulator circuit using a mathematical model of the voltage regulator circuit, wherein simulating the voltage regulator circuit includes simulating a voltage with a voltage source model; simulating ramping up or ramping down of current in the voltage regulator circuit; and simulating effects of output inductance on the voltage regulator circuit with a model of an output inductor. **Peil** teaches simulating a voltage regulator circuit using a mathematical model of the voltage regulator circuit, wherein simulating the voltage regulator circuit includes simulating a voltage with a voltage source model; simulating ramping up or ramping down of current in the voltage regulator circuit;

and simulating effects of output inductance on the voltage regulator circuit with a model of an output inductor (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the voltage and the effects of the output impedance on voltage allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included simulating a voltage regulator circuit using a mathematical model of the voltage regulator circuit, wherein simulating the voltage regulator circuit included simulating a voltage with a voltage source model; simulating ramping up or ramping down of current in the voltage regulator circuit; and simulating effects of output inductance on the voltage regulator circuit with a model of an output inductor, as simulating the voltage and the effects of the output impedance on voltage would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach simulating ramping up or ramping down of current in the voltage regulator circuit with a model of a slew inductor. **Hanf et al.** teaches simulating ramping up or ramping down of current in the voltage regulator circuit with a model of a slew inductor (CL17, L51 to CL18, L29), as by control of slew rate, radio frequency interference signal suppression can be directly influenced (CL18, L12-15). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Hanf et al.** that included simulating ramping up or ramping down of current in the voltage regulator circuit with a model of a slew inductor, as by control of slew rate, radio frequency interference signal suppression could be directly influenced.

4.2 As per Claim 2, **Chen et al., Peil** and **Hanf et al.** teach the system of claim 1. **Chen et al.** does not expressly teach that the decoupling components are capacitors, and wherein characteristics of each of the capacitors includes a rated capacitance value, a mounted inductance value, and an equivalent series resistance (ESR) value. **Peil** teaches that the decoupling components are capacitors, and wherein characteristics of each of the capacitors includes a rated capacitance value, a mounted inductance value, and an equivalent series resistance (ESR) value (Fig 7A; CL2, L46 to CL3, L6; CL12, L33 to CL13, L15; CL13, L4-15), as the voltage drop of the supply voltage is determined by the resistance of the capacitor and the series impedance of the bus bar consisting of inductance and resistance (CL12, L47-56). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included the decoupling components being capacitors, and wherein characteristics of each of the capacitors included a rated capacitance value, a mounted inductance value, and an equivalent series resistance (ESR) value, as the voltage drop of the supply voltage would be determined by the resistance of the capacitor and the series impedance of the bus bar consisting of inductance and resistance.

5. Claims 3, 6, 7, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and **Hanf et al.** (U.S. Patent 6,438,462), and further in view of **Brown** (U.S. Patent 5,960,207) and **Chan** (U.S. Patent 6,466,898).

5.1 As per Claim 3, **Chen et al., Peil** and **Hanf et al.** teach the system of claim 2. **Chen et al.** does not expressly teach that the computer system is further configured to obtain an estimate of a bulk capacitance value for the power distribution system; and refine the bulk capacitance value based on results obtained during the cyclical simulation. **Brown** teaches that the computer system is further configured to obtain an estimate of a bulk capacitance value for the power distribution system; and refine the bulk capacitance value based on results obtained during the cyclical simulation (CL6, L14-21), as the output voltage and the amount of filtering are set by the value of the bulk capacitance in relation to load current and the bulk capacitance decreases the voltage ripple (CL6, L16-21). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Brown** that included the computer system further configured to obtain an estimate of a bulk capacitance value for the power distribution system; and refine the bulk capacitance value based on results obtained during the cyclical simulation, as the output voltage and the amount of filtering would be set by the value of the bulk capacitance in relation to load current and the bulk capacitance would decrease the voltage ripple.

Chen et al. does not expressly teach that the computer system is further configured to perform a cyclical simulation of the power distribution system, wherein the cyclical simulation comprises simulating the operation of the power distribution system over a plurality of clock cycles. **Chan** teaches that the computer system is further configured to perform a cyclical simulation of the power distribution system, wherein the cyclical simulation comprises simulating the operation of the power distribution system over a plurality of clock cycles (CL1, L64-67; Fig 4; Fig 9; CL7, L47-52), as cycle based simulation allows trading off accuracy with

speed and reduce design verification time (CL1, L64-67). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Chan** that included the computer system further configured to perform a cyclical simulation of the power distribution system, wherein the cyclical simulation comprised simulating the operation of the power distribution system over a plurality of clock cycles, as cycle based simulation would allow trading off accuracy with speed and reduce design verification time.

5.2 As per Claim 6, **Chen et al., Peil, Hanf et al., Brown** and **Chan** teach the system of claim 3. **Chen et al.** does not expressly teach that the computer system is configured to simulate an output resistor of the voltage regulator circuit, wherein simulating the output resistor simulates effects of resistance between the output of the voltage regulator circuit and a load coupled to the voltage regulator circuit. **Peil** teaches that the computer system is configured to simulate an output resistor of the voltage regulator circuit, wherein simulating the output resistor simulates effects of resistance between the output of the voltage regulator circuit and a load coupled to the voltage regulator circuit (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the output resistor and the effects of resistance between the output of the voltage regulator circuit and a load coupled to the voltage regulator circuit allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included computer system configured to simulate an output resistor of the voltage regulator circuit, wherein simulating the

output resistor simulated effects of resistance between the output of the voltage regulator circuit and a load coupled to the voltage regulator circuit, as simulating the output resistor and the effects of resistance between the output of the voltage regulator circuit and a load coupled to the voltage regulator circuit would allow identification of the transient response of the voltage regulator under various conditions.

5.3 As per Claim 7, **Chen et al., Peil, Hanf et al., Brown** and **Chan** teach the system of claim 3. **Chen et al.** does not expressly teach that the computer system is configured to simulate the effects of equivalent series resistance of a capacitor in the voltage regulator circuit with a model of a decoupling resistor. **Peil** teaches that the computer system is configured to simulate the effects of equivalent series resistance of a capacitor in the voltage regulator circuit with a model of a decoupling resistor (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the effects of equivalent series resistance of a capacitor in the voltage regulator circuit with a model of a decoupling resistor allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included computer system configured to simulate the effects of equivalent series resistance of a capacitor in the voltage regulator circuit with a model of a decoupling resistor, as simulating the effects of equivalent series resistance of a capacitor in the voltage regulator circuit with a model of a decoupling resistor would allow identification of the transient response of the voltage regulator under various conditions.

Per Claim 11: **Chen et al.** teaches that the system is further configured to calculate one or more electrical characteristic values at one or more specified physical locations within the power distribution system (Page 100, CL1, Para 1).

Per Claim 12: **Chen et al.** teaches that the system is further configured to generate a resultant bill of goods, the bill of goods including a specific quantity of each of the selected decoupling components and information concerning location of physical placement of the selected decoupling components within the power distribution system (Page 99, CL1, Para 1; Page 99, CL2, Para 1).

6. Claims 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and **Hanf et al.** (U.S. Patent 6,438,462), and further in view of **Brown** (U.S. Patent 5,960,207), **Chan** (U.S. Patent 6,466,898) and **Chun et al.** ("Investigation of voltage regulation stability of static synchronous compensator in power system", IEEE, January 2000).

6.1 As per Claim 4, **Chen et al., Peil, Hanf et al., Brown** and **Chan** teach the system of claim 3. **Chen et al.** does not expressly teach that the computer system is further configured to analyze a transient response of the power distribution system during the cyclical simulation. **Chun et al.** teaches that the computer system is further configured to analyze a transient response of the power distribution system during the cyclical simulation (Page 2643, Fig 4 and 5;

Page 2644, Fig 6 and 9; Page 2644, CL1, Para 1; Page 2645, Fig 12 and 13), as the transient response indicates the speed of response as a function of time and transient gain (Page 2644, CL2, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Chun et al.** that included the computer system further configured to analyze a transient response of the power distribution system during the cyclical simulation, as the transient response would indicate the speed of response as a function of time and transient gain.

6.2 As per Claim 5, **Chen et al., Peil, Hanf et al., Brown, Chan** and **Chun et al.** teach the system of claim 4. **Chen et al.** does not expressly teach that the computer system is further configured to analyze stability of the power distribution system during the cyclical simulation. **Chun et al.** teaches that the computer system is further configured to analyze stability of the power distribution system during the cyclical simulation. (Page 2645, Fig 10; Page 2646, Fig 14 and 15; Page 2647, Fig 17; Page 2645,CL1, Para 1), as the power distribution system has resonance characteristics and in systems with low resonant frequency the transient gain must be reduced to keep stability in the voltage (Page 2645, CL1, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Chun et al.** that included the computer system further configured to analyze stability of the power distribution system during the cyclical simulation, as the power distribution system would have resonance characteristics and in systems with low resonant frequency the transient gain must be reduced to keep stability in the voltage.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and **Hanf et al.** (U.S. Patent 6,438,462), and further in view of **Brown** (U.S. Patent 5,960,207), **Chan** (U.S. Patent 6,466,898), **Skelton et al.** (U.S. Patent 6,147,478) and **Smith** ("Packaging and power distribution design considerations for sun Microsystems desktop workstation", IEEE, 1997).

7.1 As per Claim 8, **Chen et al., Peil, Hanf et al., Brown** and **Chan** teach the system of claim 3. **Chen et al.** also teaches the known system parameters for the power distribution system (Page 99, CL1, Para 3; Page 100, CL1, Para 1); comprising one or more of the following:

one or more power supply characteristics (Page 100, CL1, Para 2);

physical location constraints (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 3); or

weighting factors (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 3).

Chen et al. does not expressly teach that the known system parameters for the power distribution system comprise load characteristics and one or more voltage regulator circuit characteristics. **Peil** teaches that the known system parameters for the power distribution system comprise load characteristics and one or more voltage regulator circuit characteristics (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating load characteristics and one or more voltage regulator circuit characteristics allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included the known system parameters for the power distribution system comprising load characteristics and one or more voltage regulator circuit characteristics, as simulating load characteristics and one or more voltage regulator circuit characteristics would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach that the known system parameters for the power distribution system comprise allowable voltage ripple. **Skelton et al.** teaches that the known system parameters for the power distribution system comprise allowable voltage ripple (CL1, L29-31), as providing low ripple voltage to electronic systems avoids unstable and unpredictable operation (CL1, L29-31; CL3, L56-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Skelton et al.** that included the known system parameters for the power distribution system comprising allowable voltage ripple, as providing low ripple voltage to electronic systems would avoid unstable and unpredictable operation.

Chen et al. does not expressly teach that the known system parameters for the power distribution system comprise total current consumption. **Hanf et al.** teaches that the known system parameters for the power distribution system comprise total current consumption (CL2, L10-12), as the electronic system should minimize total current consumption during times of relative operational inactivity (CL2, L10-12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Hanf et al.** that included the known system parameters for the power distribution

system comprising total current consumption, the electronic system should minimize total current consumption during times of relative operational inactivity.

Chen et al. does not expressly teach that the known system parameters for the power distribution system comprise a frequency range for a target impedance of the power distribution system. **Smith** teaches that the known system parameters for the power distribution system comprise a frequency range for a target impedance of the power distribution system (Page 20, Para 2 and 3), as the power distribution system must deliver current to the processor at or near the target impedance at all frequencies from DC to several times the clock frequency (Page 20, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Smith** that included the known system parameters for the power distribution system comprising a frequency range for a target impedance of the power distribution system, as the power distribution system must deliver current to the processor at or near the target impedance at all frequencies from DC to several times the clock frequency.

8. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and **Hanf et al.** (U.S. Patent 6,438,462), and further in view of **Brown** (U.S. Patent 5,960,207), **Chan** (U.S. Patent 6,466,898) and **Schutz** (U.S. Patent 5,444,298).

8.1 As per Claim 9, **Chen et al., Peil, Hanf et al., Brown** and **Chan** teach the system of claim 3. **Chen et al.** does not expressly teach that the voltage regulator circuit is configured to receive a first voltage as an input, and to output a second voltage, wherein the first voltage and the second voltage are not identical. **Schutz** teaches that the voltage regulator circuit is configured to receive a first voltage as an input, and to output a second voltage, wherein the first voltage and the second voltage are not identical (CL1, L11-15; CL2, L11-19), as the lower transistor dimensions and higher density require lower operating voltage of approximately 3.3 volts or lower in stead of 5 volts, in order to prevent device failure and decrease power consumption (CL1, L39-46). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Schutz** that included the voltage regulator circuit configured to receive a first voltage as an input, and to output a second voltage, wherein the first voltage and the second voltage would not be identical, as the lower transistor dimensions and higher density would require lower operating voltage of approximately 3.3 volts or lower in stead of 5 volts, in order to prevent device failure and decrease power consumption.

8.2 As per Claim 10, **Chen et al., Peil, Hanf et al., Brown, Chan** and **Schutz** teach the system of claim 9. **Chen et al.** does not expressly teach that the mathematical model of the voltage regulator circuit is a simplified model. **Peil** teaches that the mathematical model of the voltage regulator circuit is a simplified model (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), because as per **Chan**, simplified model of the voltage regulator reduces the design verification time (CL1, L65-67). It would have been obvious to one of ordinary skill in the art at

the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included the mathematical model of the voltage regulator circuit being a simplified model, as simplified model of the voltage regulator reduces the design verification time.

Chen et al. does not expressly teach that the voltage regulator circuit is a switching voltage regulator. **Hanf et al.** teaches that the voltage regulator circuit is a switching voltage regulator (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as a switching mode voltage regulator can be activated and deactivated by means of a control signal (CL5, L25-27). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Hanf et al.** that included the voltage regulator circuit being a switching voltage regulator, as a switching mode voltage regulator could be activated and deactivated by means of a control signal.

9. Claims 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and further in view of **Brown** (U.S. Patent 5,960,207), **Smith** ("Packaging and power distribution design considerations for sun Microsystems desktop workstation", IEEE, 1997) and **Chan** (U.S. Patent 6,466,898).

9.1 As per Claim 13, **Chen et al.** teaches a method for determining a specific quantity and physical location of decoupling components within a power distribution system (Page 99, CL1, Para 1; Page 99, CL2, Para 1); the method comprising:

selecting decoupling components from a database, wherein the database includes characteristic values for a plurality of different decoupling components (Page 99, CL1, Para 1; Page 99, CL2, Para 1; Page 100, CL1, Para 1); and

selecting one or more of the different decoupling components based on one or more electrical characteristic values for each of the decoupling components (Abstract, L10-14; Page 99, CL1, Para 1; Page 99, CL2, Para 1; Page 100, CL1, Para 1).

Chen et al. does not expressly teach determining a target impedance for the power distribution system. **Smith** teaches determining a target impedance for the power distribution system (Page 20, Para 2 and 3), as the power distribution system must deliver current to the processor at or near the target impedance at all frequencies from DC to several times the clock frequency (Page 20, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Smith** that included determining a target impedance for the power distribution system, as the power distribution system must deliver current to the processor at or near the target impedance at all frequencies from DC to several times the clock frequency.

Chen et al. does not expressly teach simulating the operation of the power distribution system, wherein the power distribution system includes a voltage regulator circuit coupled to a load. **Peil** teaches simulating the operation of the power distribution system, wherein the power distribution system includes a voltage regulator circuit coupled to a load (Fig 2; CL7, L11-30; CL8, L4-13; CL8, L65-68; CL9, L33-40, L61-65; CL12, L33 to CL13, L15; CL13, L32-48; Fig 6), as the voltage regulation stabilizes the output voltage to within allowable tolerance (CL8,

L10-12; CL12, L59-64) and simulating the voltage regulator allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Peil** that included simulating the operation of the power distribution system, wherein the power distribution system included a voltage regulator circuit coupled to a load, as the voltage regulation would stabilize the output voltage to within allowable tolerance; and simulating the voltage regulator would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach simulating the operation of the voltage regulator circuit using a model of the voltage regulator circuit. **Peil** teaches simulating the operation of the voltage regulator circuit using a model of the voltage regulator circuit (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the operation of the voltage regulator circuit using a model of the voltage regulator circuit allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Peil** that included simulating the operation of the voltage regulator circuit using a model of the voltage regulator circuit, as simulating the operation of the voltage regulator circuit using a model of the voltage regulator circuit would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach obtaining an estimate of a bulk capacitance value for the power distribution system; refining the bulk capacitance value based on results obtained during the cyclical simulation; and selecting one or more of the different decoupling components

based on the bulk capacitance obtained during the simulating the operation of the power distribution system. **Brown** teaches obtaining an estimate of a bulk capacitance value for the power distribution system; refining the bulk capacitance value based on results obtained during the cyclical simulation; and selecting one or more of the different decoupling components based on the bulk capacitance obtained during the simulating the operation of the power distribution system (CL6, L14-21), as the output voltage and the amount of filtering are set by the value of the bulk capacitance in relation to load current and the bulk capacitance decreases the voltage ripple (CL6, L16-21). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Brown** that included obtaining an estimate of a bulk capacitance value for the power distribution system; refining the bulk capacitance value based on results obtained during the cyclical simulation; and selecting one or more of the different decoupling components based on the bulk capacitance obtained during the simulating the operation of the power distribution system, as the output voltage and the amount of filtering would be set by the value of the bulk capacitance in relation to load current and the bulk capacitance would decrease the voltage ripple.

Chen et al. does not expressly teach performing a cyclical simulation of the power distribution system, wherein the cyclical simulation includes simulating the operation of the power distribution system for a plurality of clock cycles. **Chan** teaches performing a cyclical simulation of the power distribution system, wherein the cyclical simulation includes simulating the operation of the power distribution system for a plurality of clock cycles (CL1, L64-67; Fig 4; Fig 9; CL7, L47-52), as cycle based simulation allows trading off accuracy with speed and reduce design verification time (CL1, L64-67). It would have been obvious to one of ordinary

skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Chan** that included performing a cyclical simulation of the power distribution system, wherein the cyclical simulation includes simulating the operation of the power distribution system for a plurality of clock cycles, as cycle based simulation would allow trading off accuracy with speed and reduce design verification time.

9.2 As per Claim 16, **Chen et al., Peil, Brown**, **Smith** and **Chan** teach the method of claim 13. **Chen et al.** does not expressly teach that the decoupling components are capacitors, and wherein characteristics of each of the capacitors includes a rated capacitance value, a mounted inductance value, and an equivalent series resistance (ESR) value. **Peil** teaches that the decoupling components are capacitors, and wherein characteristics of each of the capacitors includes a rated capacitance value, a mounted inductance value, and an equivalent series resistance (ESR) value (Fig 7A; CL2, L46 to CL3, L6; CL12, L33 to CL13, L15; CL13, L4-15), as the voltage drop of the supply voltage is determined by the resistance of the capacitor and the series impedance of the bus bar consisting of inductance and resistance (CL12, L47-56). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Peil** that included the decoupling components being capacitors, and wherein characteristics of each of the capacitors included a rated capacitance value, a mounted inductance value, and an equivalent series resistance (ESR) value, as the voltage drop of the supply voltage would be determined by the resistance of the capacitor and the series impedance of the bus bar consisting of inductance and resistance.

10. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and further in view of **Brown** (U.S. Patent 5,960,207), **Smith** ("Packaging and power distribution design considerations for sun Microsystems desktop workstation", IEEE, 1997), **Chan** (U.S. Patent 6,466,898) and **Chun et al.** ("Investigation of voltage regulation stability of static synchronous compensator in power system", IEEE, January 2000).

10.1 As per Claim 14, **Chen et al., Peil, Brown, Smith** and **Chan** teach the method of claim 13. **Chen et al.** does not expressly teach that the simulating the operation of the power distribution system includes analyzing at least one transient response during the cyclical simulation. **Chun et al.** teaches that the simulating the operation of the power distribution system includes analyzing at least one transient response during the cyclical simulation (Page 2643, Fig 4 and 5; Page 2644, Fig 6 and 9; Page 2644, CL1, Para 1; Page 2645, Fig 12 and 13), as the transient response indicates the speed of response as a function of time and transient gain (Page 2644, CL2, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Chun et al.** that included the simulating the operation of the power distribution system including analyzing at least one transient response during the cyclical simulation, as the transient response would indicate the speed of response as a function of time and transient gain.

10.2 As per Claim 15, **Chen et al., Peil, Brown, Smith, Chan** and **Chun et al.** teach the system of claim 14. **Chen et al.** does not expressly teach that the simulating the operation of the power distribution system includes analyzing the stability of the power distribution system. **Chun et al.** teaches that the simulating the operation of the power distribution system includes analyzing the stability of the power distribution system (Page 2645, Fig 10; Page 2646, Fig 14 and 15; Page 2647, Fig 17; Page 2645, CL1, Para 1), as the power distribution system has resonance characteristics and in systems with low resonant frequency the transient gain must be reduced to keep stability in the voltage (Page 2645, CL1, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Chun et al.** that included the simulating the operation of the power distribution system including analyzing the stability of the power distribution system, as the power distribution system would have resonance characteristics and in systems with low resonant frequency the transient gain must be reduced to keep stability in the voltage.

11. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and **Hanf et al.** (U.S. Patent 6,438,462), and further in view of **Brown** (U.S. Patent 5,960,207), **Chan** (U.S. Patent 6,466,898) and **Smith** ("Packaging and power distribution design considerations for sun Microsystems desktop workstation", IEEE, 1997).

11.1 As per Claim 17, **Chen et al., Peil, Brown**, **Smith** and **Chan** teach the method of claim 13. **Chen et al.** does not expressly teach that the model of the voltage regulator circuit is a mathematical model, wherein the mathematical model comprises a voltage source model, wherein the voltage source model is configured for simulating a voltage source for the power distribution system; and an output inductor model, wherein the output inductor model is configured for simulating effects of output inductance on the voltage regulator circuit. **Peil** teaches that the model of the voltage regulator circuit is a mathematical model, wherein the mathematical model comprises a voltage source model, wherein the voltage source model is configured for simulating a voltage source for the power distribution system; and an output inductor model, wherein the output inductor model is configured for simulating effects of output inductance on the voltage regulator circuit (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the voltage and the effects of the output impedance on voltage allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Peil** that included the model of the voltage regulator circuit being a mathematical model, wherein the mathematical model comprised a voltage source model, wherein the voltage source model was configured for simulating a voltage source for the power distribution system; and an output inductor model, wherein the output inductor model was configured for simulating effects of output inductance on the voltage regulator circuit, as simulating the voltage and the effects of the output impedance on voltage would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach a slew inductor model, wherein the slew inductor model is configured for simulating a ramping up or a ramping down of current in the voltage regulator circuit. **Hanf et al.** teaches a slew inductor model, wherein the slew inductor model is configured for simulating a ramping up or a ramping down of current in the voltage regulator circuit (CL17, L51 to CL18, L29), as by control of slew rate, radio frequency interference signal suppression can be directly influenced (CL18, L12-15). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Hanf et al.** that included a slew inductor model, wherein the slew inductor model was configured for simulating a ramping up or a ramping down of current in the voltage regulator circuit, as by control of slew rate, radio frequency interference signal suppression could be directly influenced.

Chen et al. does not expressly teach a decoupling resistor model, wherein the decoupling resistor model is configured to simulate the effects of an equivalent series resistance of a capacitor in the voltage regulator circuit. **Peil** teaches a decoupling resistor model, wherein the decoupling resistor model is configured to simulate the effects of an equivalent series resistance of a capacitor in the voltage regulator circuit (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the effects of equivalent series resistance of a capacitor in the voltage regulator circuit with a model of a decoupling resistor allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Peil** that included a decoupling resistor model, wherein the decoupling resistor model is configured to simulate the effects of an equivalent

series resistance of a capacitor in the voltage regulator circuit, as simulating the effects of equivalent series resistance of a capacitor in the voltage regulator circuit with a model of a decoupling resistor would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach an output resistor model, wherein the output resistor model is configured for simulating effects of resistance between an output of the voltage regulator circuit and the load. **Peil** teaches an output resistor model, wherein the output resistor model is configured for simulating effects of resistance between an output of the voltage regulator circuit and the load (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the output resistor and the effects of resistance between the output of the voltage regulator circuit and a load allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Peil** that included an output resistor model, wherein the output resistor model is configured for simulating effects of resistance between an output of the voltage regulator circuit and the load, as simulating the output resistor and the effects of resistance between the output of the voltage regulator circuit and a load would allow identification of the transient response of the voltage regulator under various conditions.

11.2 As per Claim 18, **Chen et al., Peil, Hanf et al., Brown, Smith** and **Chan** teach the method of claim 17. **Chen et al.** does not expressly teach that the mathematical model of the voltage regulator circuit is a simplified model. **Peil** teaches that the mathematical model of the

voltage regulator circuit is a simplified model (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), because as per **Chan**, simplified model of the voltage regulator reduces the design verification time (CL1, L65-67). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Peil** that included the mathematical model of the voltage regulator circuit being a simplified model, as simplified model of the voltage regulator reduces the design verification time.

Chen et al. does not expressly teach that the voltage regulator circuit is a switching voltage regulator. **Hanf et al.** teaches that the voltage regulator circuit is a switching voltage regulator (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as a switching mode voltage regulator can be activated and deactivated by means of a control signal (CL5, L25-27). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Hanf et al.** that included the voltage regulator circuit being a switching voltage regulator, as a switching mode voltage regulator could be activated and deactivated by means of a control signal.

12. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and **Hanf et al.** (U.S. Patent 6,438,462), and further in view of **Brown** (U.S. Patent 5,960,207), **Chan** (U.S. Patent 6,466,898), **Smith** ("Packaging and power distribution design considerations for sun Microsystems desktop workstation", IEEE, 1997) and **O'Sullivan et al.** ("Developing decoupling methodology with SPICE for multilayered printed circuit boards", IEEE, 1998).

12.1 As per Claim 19, **Chen et al., Peil, Hanf et al., Brown**, **Smith** and **Chan** teach the method of claim 18. **Chen et al.** does not expressly teach the mathematical model of the voltage regulator circuit. **Peil** teaches the mathematical model of the voltage regulator (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the voltage regulator allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Peil** that included the mathematical model of the voltage regulator circuit, as simulating the voltage regulator circuit using a SPICE model would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach that the mathematical model of the voltage regulator circuit is a SPICE model. **O'Sullivan et al.** teaches that the mathematical model of the voltage regulator circuit is a SPICE model (Page 652, CL1, Para 2; Page 653, CL1, Para 1; Page 655, CL1, Para 3 and 4), as the SPICE model allows calculating the impedance at numerous points around the board, thus enabling the choice and quantity of the decoupling capacitors, their placement and the resulting power supply impedance to be evaluated (Page 652, CL1, Para 2); and the SPICE model has high speed of execution (Page 655, CL1, Para 4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **O'Sullivan et al.** that included the mathematical model of the voltage regulator circuit being a SPICE model, as the SPICE model would allow calculating the impedance at numerous points around the board, thus enabling the choice and

quantity of the decoupling capacitors, their placement and the resulting power supply impedance to be evaluated; and the SPICE model would have high speed of execution.

13. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and **Hanf et al.** (U.S. Patent 6,438,462), and further in view of **Brown** (U.S. Patent 5,960,207), **Chan** (U.S. Patent 6,466,898), **Smith** ("Packaging and power distribution design considerations for sun Microsystems desktop workstation", IEEE, 1997) and **Schutz** (U.S. Patent 5,444,298).

13.1 As per Claim 20, **Chen et al., Peil, Hanf et al., Brown, Smith** and **Chan** teach the method of claim 18. **Chen et al.** does not expressly teach that the voltage regulator circuit is configured to receive a first voltage as an input, and to output a second voltage, wherein the first voltage and the second voltage are not identical. **Schutz** teaches that the voltage regulator circuit is configured to receive a first voltage as an input, and to output a second voltage, wherein the first voltage and the second voltage are not identical (CL1, L11-15; CL2, L11-19), as the lower transistor dimensions and higher density require lower operating voltage of approximately 3.3 volts or lower in stead of 5 volts, in order to prevent device failure and decrease power consumption (CL1, L39-46). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Schutz** that included the voltage regulator circuit configured to receive a first voltage as an input, and to output a second voltage, wherein the first voltage and the second voltage would not be identical,

as the lower transistor dimensions and higher density would require lower operating voltage of approximately 3.3 volts or lower in stead of 5 volts, in order to prevent device failure and decrease power consumption.

14. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and **Hanf et al.** (U.S. Patent 6,438,462), and further in view of **Brown** (U.S. Patent 5,960,207), **Chan** (U.S. Patent 6,466,898), **Smith** ("Packaging and power distribution design considerations for sun Microsystems desktop workstation", IEEE, 1997) and **Skelton et al.** (U.S. Patent 6,147,478).

14.1 As per Claim 21, **Chen et al., Peil, Brown, Chan** and **Smith** teach the method of claim 13. **Chen et al.** also teaches selecting the decoupling components based on known system parameters (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 100, CL1, Para 1); the known system parameters include one or more of the following:

one or more power supply characteristics (Page 100, CL1, Para 2);

physical location constraints (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 3); or

weighting factors (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 3).

Chen et al. does not expressly teach that system parameters include load characteristics and one or more voltage regulator circuit characteristics. **Peil** teaches that system parameters

include load characteristics and one or more voltage regulator circuit characteristics (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating load characteristics and one or more voltage regulator circuit characteristics allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Peil** that included system parameters including load characteristics and one or more voltage regulator circuit characteristics, as simulating load characteristics and one or more voltage regulator circuit characteristics would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach that system parameters include allowable voltage ripple. **Skelton et al.** teaches that system parameters include allowable voltage ripple (CL1, L29-31), as providing low ripple voltage to electronic systems avoids unstable and unpredictable operation (CL1, L29-31; CL3, L56-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Skelton et al.** that included system parameters including allowable voltage ripple, as providing low ripple voltage to electronic systems would avoid unstable and unpredictable operation.

Chen et al. does not expressly teach that system parameters include total current consumption. **Hanf et al.** teaches that system parameters include total current consumption (CL2, L10-12), as the electronic system should minimize total current consumption during times of relative operational inactivity (CL2, L10-12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the

method of **Hanf et al.** that included system parameters including total current consumption, the electronic system should minimize total current consumption during times of relative operational inactivity.

Chen et al. does not expressly teach that system parameters include a frequency range for a target impedance of the power distribution system. **Smith** teaches that system parameters include a frequency range for a target impedance of the power distribution system (Page 20, Para 2 and 3), as the power distribution system must deliver current to the processor at or near the target impedance at all frequencies from DC to several times the clock frequency (Page 20, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Smith** that included system parameters including a frequency range for a target impedance of the power distribution system, as the power distribution system must deliver current to the processor at or near the target impedance at all frequencies from DC to several times the clock frequency.

Per Claim 22: **Chen et al.** teaches that the system is further configured to calculate one or more electrical characteristic values at one or more specified physical locations within the power distribution system (Page 100, CL1, Para 1).

Per Claim 23: **Chen et al.** teaches that the system is further configured to generate a resultant bill of goods, the bill of goods including a specific quantity of each of the selected decoupling components and information concerning location of physical placement of the

selected decoupling components within the power distribution system (Page 99, CL1, Para 1; Page 99, CL2, Para 1).

14.2 As per Claim 24, **Chen et al., Peil, Hanf et al., Brown, Chan, Smith** and **Skelton et al.** teach the method of claim 23. **Chen et al.** also teaches changing the specific quantity for any of the decoupling components selected from the database (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL1, Para 1);

recalculating placement of the decoupling components at a specific location within the power distribution system (Abstract, L10-14; Page 99, CL2, Para 1; Page 102, CL2, Para 3);

the recalculating is based upon the known system parameters for the power distribution system, electrical characteristic values for the decoupling components, and the changing specific quantity for any of the decoupling components (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 3).

Chen et al. does not expressly teach that the changing is based on the refining the bulk capacitance value. **Brown** teaches that the changing is based on the refining the bulk capacitance value (CL6, L14-21), as the output voltage and the amount of filtering are set by the value of the bulk capacitance in relation to load current and the bulk capacitance decreases the voltage ripple (CL6, L16-21). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen et al.** with the method of **Brown** that included the changing based on the refining the bulk capacitance value, as the output

voltage and the amount of filtering would be set by the value of the bulk capacitance in relation to load current and the bulk capacitance would decrease the voltage ripple.

15. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), and further in view of **Hanf et al.** (U.S. Patent 6,438,462) and **O'Sullivan et al.** ("Developing decoupling methodology with SPICE for multilayered printed circuit boards", IEEE, 1998).

15.1 As per Claim 25, **Chen et al.** teaches a system for determining decoupling components for a power distribution system (Abstract, L1-4; Page 99, CL1, Para 3); the system comprising:

a database of characteristic values for a plurality of decoupling components (Page 99, CL1, Para 3; Page 99, CL2, Para 1); and

a computer system configured to:

access the database of characteristic values for the plurality of decoupling components (Page 99, CL1, Para 3; Page 99, CL2, Para 1);

accept known system parameters for the power distribution system (Page 99, CL1, Para 3; Page 100, CL1, Para 1);

select one or more different decoupling components based on the known system parameters for the power distribution system and entries in the database (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 100, CL1, Para 1);

calculate a specific quantity for selected decoupling components, the selected decoupling components selected from the database based on known system parameters (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 4); and

determine a location of placement within the power distribution system for each of the selected decoupling components based on the known system parameters and the entries in the database (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 3).

Chen et al. does not expressly teach the power distribution system including a voltage regulator module. **Peil** teaches the power distribution system including a voltage regulator module (Fig 2; CL7, L11-30; CL8, L4-13; CL8, L65-68; CL9, L33-40, L61-65; CL12, L33 to CL13, L15; CL13, L32-48; Fig 6), as the voltage regulation stabilizes the output voltage to within allowable tolerance (CL8, L10-12; CL12, L59-64). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included the power distribution system including a voltage regulator module, as the voltage regulation would stabilize the output voltage to within allowable tolerance.

Chen et al. does not expressly teach simulating a voltage regulator, wherein simulating the voltage regulator circuit includes simulating a voltage with a voltage source model; simulating ramping up or ramping down of current in the voltage regulator circuit; and simulating effects of output inductance on the voltage regulator circuit with a model of an output inductor. **Peil** teaches simulating a voltage regulator circuit, wherein simulating the voltage

regulator circuit includes simulating a voltage with a voltage source model; simulating ramping up or ramping down of current in the voltage regulator circuit; and simulating effects of output inductance on the voltage regulator circuit with a model of an output inductor (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the voltage and the effects of the output impedance on voltage allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included simulating a voltage regulator circuit, wherein simulating the voltage regulator circuit included simulating a voltage with a voltage source model; simulating ramping up or ramping down of current in the voltage regulator circuit; and simulating effects of output inductance on the voltage regulator circuit with a model of an output inductor, as simulating the voltage and the effects of the output impedance on voltage would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach that simulating the voltage regulator circuit includes simulating a voltage with a SPICE model of a voltage source; simulating ramping up or ramping down of current in the voltage regulator circuit with a SPICE model of a slew inductor; and simulating effects of output inductance on the voltage regulator circuit with a SPICE model of an output inductor. **O'Sullivan et al.** teaches that simulating the voltage regulator circuit includes simulating a voltage with a SPICE model of a voltage source; simulating ramping up or ramping down of current in the voltage regulator circuit with a SPICE model of a slew inductor; and simulating effects of output inductance on the voltage regulator circuit with a SPICE model of an output inductor (Page 652, CL1, Para 2; Page 653, CL1, Para 1; Page 655, CL1, Para 3 and 4), as

the SPICE model allows calculating the impedance at numerous points around the board, thus enabling the choice and quantity of the decoupling capacitors, their placement and the resulting power supply impedance to be evaluated (Page 652, CL1, Para 2); and the SPICE model has high speed of execution (Page 655, CL1, Para 4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **O'Sullivan et al.** that included simulating the voltage regulator circuit including simulating a voltage with a SPICE model of a voltage source; simulating ramping up or ramping down of current in the voltage regulator circuit with a SPICE model of a slew inductor; and simulating effects of output inductance on the voltage regulator circuit with a SPICE model of an output inductor, as the SPICE model would allow calculating the impedance at numerous points around the board, thus enabling the choice and quantity of the decoupling capacitors, their placement and the resulting power supply impedance to be evaluated; and the SPICE model would have high speed of execution.

Chen et al. does not expressly teach simulating ramping up or ramping down of current in the voltage regulator circuit with a model of a slew inductor. **Hanf et al.** teaches simulating ramping up or ramping down of current in the voltage regulator circuit with a model of a slew inductor (CL17, L51 to CL18, L29), as by control of slew rate, radio frequency interference signal suppression can be directly influenced (CL18, L12-15). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Hanf et al.** that included simulating ramping up or ramping down of current in the voltage regulator circuit with a model of a slew inductor, as by control of slew rate, radio frequency interference signal suppression could be directly influenced.

15.2 As per Claim 26, **Chen et al., Peil, Hanf et al.** and **O'Sullivan et al.** teach the system of claim 1. **Chen et al.** does not expressly teach that the decoupling components are capacitors, and wherein characteristics of each of the capacitors includes a rated capacitance value, a mounted inductance value, and an equivalent series resistance (ESR) value. **Peil** teaches that the decoupling components are capacitors, and wherein characteristics of each of the capacitors includes a rated capacitance value, a mounted inductance value, and an equivalent series resistance (ESR) value (Fig 7A; CL2, L46 to CL3, L6; CL12, L33 to CL13, L15; CL13, L4-15), as the voltage drop of the supply voltage is determined by the resistance of the capacitor and the series impedance of the bus bar consisting of inductance and resistance (CL12, L47-56). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included the decoupling components being capacitors, and wherein characteristics of each of the capacitors included a rated capacitance value, a mounted inductance value, and an equivalent series resistance (ESR) value, as the voltage drop of the supply voltage would be determined by the resistance of the capacitor and the series impedance of the bus bar consisting of inductance and resistance.

16. Claims 27, 30, 31, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), **Hanf et al.** (U.S. Patent 6,438,462), and **O'Sullivan et al.** ("Developing decoupling methodology with SPICE for

multilayered printed circuit boards", IEEE, 1998), and further in view of **Brown** (U.S. Patent 5,960,207) and **Chan** (U.S. Patent 6,466,898).

16.1 As per Claim 27, **Chen et al., Peil, Hanf et al.** and **O'Sullivan et al.** teach the system of claim 26. **Chen et al.** does not expressly teach that the computer system is further configured to obtain an estimate of a bulk capacitance value for the power distribution system; and refine the bulk capacitance value based on results obtained during the cyclical simulation. **Brown** teaches that the computer system is further configured to obtain an estimate of a bulk capacitance value for the power distribution system; and refine the bulk capacitance value based on results obtained during the cyclical simulation (CL6, L14-21), as the output voltage and the amount of filtering are set by the value of the bulk capacitance in relation to load current and the bulk capacitance decreases the voltage ripple (CL6, L16-21). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Brown** that included the computer system further configured to obtain an estimate of a bulk capacitance value for the power distribution system; and refine the bulk capacitance value based on results obtained during the cyclical simulation, as the output voltage and the amount of filtering would be set by the value of the bulk capacitance in relation to load current and the bulk capacitance would decrease the voltage ripple.

Chen et al. does not expressly teach that the computer system is further configured to perform a cyclical simulation of the power distribution system, wherein the cyclical simulation comprises simulating the operation of the power distribution system over a plurality of clock cycles. **Chan** teaches that the computer system is further configured to perform a cyclical

simulation of the power distribution system, wherein the cyclical simulation comprises simulating the operation of the power distribution system over a plurality of clock cycles (CL1, L64-67; Fig 4; Fig 9; CL7, L47-52), as cycle based simulation allows trading off accuracy with speed and reduce design verification time (CL1, L64-67). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Chan** that included the computer system further configured to perform a cyclical simulation of the power distribution system, wherein the cyclical simulation comprised simulating the operation of the power distribution system over a plurality of clock cycles, as cycle based simulation would allow trading off accuracy with speed and reduce design verification time.

16.2 As per Claim 30, **Chen et al., Peil, Hanf et al., O'Sullivan et al., Brown** and **Chan** teach the system of claim 27. **Chen et al.** does not expressly teach that the computer system is configured to simulate the effects of an output resistance from a load coupled to the voltage regulator circuit. **Peil** teaches that the computer system is configured to simulate the effects of an output resistance from a load coupled to the voltage regulator circuit (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the output resistor and the effects of resistance between the output of the voltage regulator circuit and a load coupled to the voltage regulator circuit allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included the computer system being configured to simulate the effects of an output

resistance from a load coupled to the voltage regulator circuit, as simulating the output resistor and the effects of resistance between the output of the voltage regulator circuit and a load coupled to the voltage regulator circuit would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach that the computer system is configured to simulate the effects of an output resistance from a load coupled to the voltage regulator circuit using a SPICE model of an output resistor. **O'Sullivan et al.** teaches that the computer system is configured to simulate the effects of an output resistance from a load coupled to the voltage regulator circuit using a SPICE model of an output resistor (Page 652, CL1, Para 2; Page 653, CL1, Para 1; Page 655, CL1, Para 3 and 4), as the SPICE model allows calculating the impedance at numerous points around the board, thus enabling the choice and quantity of the decoupling capacitors, their placement and the resulting power supply impedance to be evaluated (Page 652, CL1, Para 2); and the SPICE model has high speed of execution (Page 655, CL1, Para 4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **O'Sullivan et al.** that included the computer system being configured to simulate the effects of an output resistance from a load coupled to the voltage regulator circuit using a SPICE model of an output resistor, as the SPICE model would allow calculating the impedance at numerous points around the board, thus enabling the choice and quantity of the decoupling capacitors, their placement and the resulting power supply impedance to be evaluated; and the SPICE model would have high speed of execution.

16.3 As per Claim 31, **Chen et al., Peil, Hanf et al., O'Sullivan et al., Brown** and **Chan** teach the system of claim 30. **Chen et al.** does not expressly teach that the computer system is configured to simulate the effects of an equivalent series resistance from a capacitor in the voltage regulator circuit using a model of a decoupling resistor. **Peil** teaches that the computer system is configured to simulate the effects of an equivalent series resistance from a capacitor in the voltage regulator circuit using a model of a decoupling resistor (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating the effects of equivalent series resistance of a capacitor in the voltage regulator circuit with a model of a decoupling resistor allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included the computer system configured to simulate the effects of an equivalent series resistance from a capacitor in the voltage regulator circuit using a model of a decoupling resistor, as simulating the effects of equivalent series resistance of a capacitor in the voltage regulator circuit with a model of a decoupling resistor would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach that the computer system is configured to simulate the effects of an equivalent series resistance from a capacitor in the voltage regulator circuit using a SPICE model of a decoupling resistor. **O'Sullivan et al.** teaches that the computer system is configured to simulate the effects of an equivalent series resistance from a capacitor in the voltage regulator circuit using a SPICE model of a decoupling resistor (Page 652, CL1, Para 2; Page 653, CL1, Para 1; Page 655, CL1, Para 3 and 4), as the SPICE model allows calculating

the impedance at numerous points around the board, thus enabling the choice and quantity of the decoupling capacitors, their placement and the resulting power supply impedance to be evaluated (Page 652, CL1, Para 2); and the SPICE model has high speed of execution (Page 655, CL1, Para 4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **O'Sullivan et al.** that included the computer system configured to simulate the effects of an equivalent series resistance from a capacitor in the voltage regulator circuit using a SPICE model of a decoupling resistor, as the SPICE model would allow calculating the impedance at numerous points around the board, thus enabling the choice and quantity of the decoupling capacitors, their placement and the resulting power supply impedance to be evaluated; and the SPICE model would have high speed of execution.

Per Claim 35: **Chen et al.** teaches that the system is further configured to calculate one or more electrical characteristic values at one or more specified physical locations within the power distribution system (Page 100, CL1, Para 1).

Per Claim 36: **Chen et al.** teaches that the system is further configured to generate a resultant bill of goods, the bill of goods including a specific quantity of each of the selected decoupling components and information concerning location of physical placement of the selected decoupling components within the power distribution system (Page 99, CL1, Para 1; Page 99, CL2, Para 1).

17. Claims 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), **Hanf et al.** (U.S. Patent 6,438,462) and **O'Sullivan et al.** ("Developing decoupling methodology with SPICE for multilayered printed circuit boards", IEEE, 1998), and further in view of **Brown** (U.S. Patent 5,960,207), **Chan** (U.S. Patent 6,466,898) and **Chun et al.** ("Investigation of voltage regulation stability of static synchronous compensator in power system", IEEE, January 2000).

17.1 As per Claim 28, **Chen et al., Peil, Hanf et al., O'Sullivan et al., Brown** and **Chan** teach the system of claim 27. **Chen et al.** does not expressly teach that the computer system is further configured to analyze a transient response of the power distribution system during the cyclical simulation. **Chun et al.** teaches that the computer system is further configured to analyze a transient response of the power distribution system during the cyclical simulation (Page 2643, Fig 4 and 5; Page 2644, Fig 6 and 9; Page 2644, CL1, Para 1; Page 2645, Fig 12 and 13), as the transient response indicates the speed of response as a function of time and transient gain (Page 2644, CL2, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Chun et al.** that included the computer system further configured to analyze a transient response of the power distribution system during the cyclical simulation, as the transient response would indicate the speed of response as a function of time and transient gain.

17.2 As per Claim 29, **Chen et al., Peil, Hanf et al., O'Sullivan et al., Brown, Chan** and **Chun et al.** teach the system of claim 28. **Chen et al.** does not expressly teach that the computer system is further configured to analyze stability of the power distribution system during the cyclical simulation. **Chun et al.** teaches that the computer system is further configured to analyze stability of the power distribution system during the cyclical simulation. (Page 2645, Fig 10; Page 2646, Fig 14 and 15; Page 2647, Fig 17; Page 2645,CL1, Para 1), as the power distribution system has resonance characteristics and in systems with low resonant frequency the transient gain must be reduced to keep stability in the voltage (Page 2645, CL1, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Chun et al.** that included the computer system further configured to analyze stability of the power distribution system during the cyclical simulation, as the power distribution system would have resonance characteristics and in systems with low resonant frequency the transient gain must be reduced to keep stability in the voltage.

18. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), **Hanf et al.** (U.S. Patent 6,438,462), and **O'Sullivan et al.** ("Developing decoupling methodology with SPICE for multilayered printed circuit boards", IEEE, 1998), and further in view of **Brown** (U.S. Patent 5,960,207), **Chan** (U.S. Patent 6,466,898), **Skelton et al.** (U.S. Patent 6,147,478) and **Smith** ("Packaging and power distribution design considerations for sun Microsystems desktop workstation", IEEE, 1997).

18.1 As per Claim 32, **Chen et al., Peil, Hanf et al., O'Sullivan et al., Brown** and **Chan** teach the system of claim 27. **Chen et al.** also teaches the known system parameters for the power distribution system (Page 99, CL1, Para 3; Page 100, CL1, Para 1) comprise one or more of the following:

one or more power supply characteristics (Page 100, CL1, Para 2);

physical location constraints (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 3); or

weighting factors (Abstract, L10-14; Page 99, CL1, Para 3; Page 99, CL2, Para 1; Page 102, CL2, Para 3).

Chen et al. does not expressly teach that the known system parameters for the power distribution system comprise load characteristics and one or more voltage regulator circuit characteristics. **Peil** teaches that the known system parameters for the power distribution system comprise load characteristics and one or more voltage regulator circuit characteristics (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as simulating load characteristics and one or more voltage regulator circuit characteristics allows identification of the transient response of the voltage regulator under various conditions (Fig 7B; CL13, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included the known system parameters for the power distribution system comprising load characteristics and one or more voltage regulator circuit characteristics, as simulating load characteristics and one or more voltage regulator circuit

characteristics would allow identification of the transient response of the voltage regulator under various conditions.

Chen et al. does not expressly teach that the known system parameters for the power distribution system comprise allowable voltage ripple. **Skelton et al.** teaches that the known system parameters for the power distribution system comprise allowable voltage ripple (CL1, L29-31), as providing low ripple voltage to electronic systems avoids unstable and unpredictable operation (CL1, L29-31; CL3, L56-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Skelton et al.** that included the known system parameters for the power distribution system comprising allowable voltage ripple, as providing low ripple voltage to electronic systems would avoid unstable and unpredictable operation.

Chen et al. does not expressly teach that the known system parameters for the power distribution system comprise total current consumption. **Hanf et al.** teaches that the known system parameters for the power distribution system comprise total current consumption (CL2, L10-12), as the electronic system should minimize total current consumption during times of relative operational inactivity (CL2, L10-12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Hanf et al.** that included the known system parameters for the power distribution system comprising total current consumption, the electronic system should minimize total current consumption during times of relative operational inactivity.

Chen et al. does not expressly teach that the known system parameters for the power distribution system comprise a frequency range for a target impedance of the power distribution

system. **Smith** teaches that the known system parameters for the power distribution system comprise a frequency range for a target impedance of the power distribution system (Page 20, Para 2 and 3), as the power distribution system must deliver current to the processor at or near the target impedance at all frequencies from DC to several times the clock frequency (Page 20, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Smith** that included the known system parameters for the power distribution system comprising a frequency range for a target impedance of the power distribution system, as the power distribution system must deliver current to the processor at or near the target impedance at all frequencies from DC to several times the clock frequency.

19. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998) in view of **Peil** (U.S. Patent 4,806,937), **Hanf et al.** (U.S. Patent 6,438,462) and **O'Sullivan et al.** ("Developing decoupling methodology with SPICE for multilayered printed circuit boards", IEEE, 1998), and further in view of **Brown** (U.S. Patent 5,960,207), **Chan** (U.S. Patent 6,466,898) and **Schutz** (U.S. Patent 5,444,298).

19.1 As per Claim 33, **Chen et al., Peil, Hanf et al., O'Sullivan et al., Brown** and **Chan** teach the system of claim 27. **Chen et al.** does not expressly teach that the voltage regulator circuit is configured to receive a first voltage as an input, and to output a second voltage, wherein the first voltage and the second voltage are not identical. **Schutz** teaches that the voltage

regulator circuit is configured to receive a first voltage as an input, and to output a second voltage, wherein the first voltage and the second voltage are not identical (CL1, L11-15; CL2, L11-19), as the lower transistor dimensions and higher density require lower operating voltage of approximately 3.3 volts or lower in stead of 5 volts, in order to prevent device failure and decrease power consumption (CL1, L39-46). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Schutz** that included the voltage regulator circuit configured to receive a first voltage as an input, and to output a second voltage, wherein the first voltage and the second voltage would not be identical, as the lower transistor dimensions and higher density would require lower operating voltage of approximately 3.3 volts or lower in stead of 5 volts, in order to prevent device failure and decrease power consumption.

19.2 As per Claim 34, **Chen et al., Peil, Hanf et al., O'Sullivan et al., Brown, Chan** and **Schutz** teach the system of claim 9. **Chen et al.** does not expressly teach that the mathematical model of the voltage regulator circuit is a simplified model. **Peil** teaches that the mathematical model of the voltage regulator circuit is a simplified model (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), because as per **Chan**, simplified model of the voltage regulator reduces the design verification time (CL1, L65-67). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Peil** that included the mathematical model of the voltage regulator circuit being a simplified model, as simplified model of the voltage regulator reduces the design verification time.

Chen et al. does not expressly teach that the voltage regulator circuit model is a SPICE model. **O'Sullivan et al.** teaches that the voltage regulator circuit model is a SPICE model (Page 652, CL1, Para 2; Page 653, CL1, Para 1; Page 655, CL1, Para 3 and 4), as the SPICE model allows calculating the impedance at numerous points around the board, thus enabling the choice and quantity of the decoupling capacitors, their placement and the resulting power supply impedance to be evaluated (Page 652, CL1, Para 2); and the SPICE model has high speed of execution (Page 655, CL1, Para 4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **O'Sullivan et al.** that included the voltage regulator circuit model being a SPICE model, as the SPICE model would allow calculating the impedance at numerous points around the board, thus enabling the choice and quantity of the decoupling capacitors, their placement and the resulting power supply impedance to be evaluated; and the SPICE model would have high speed of execution.

Chen et al. does not expressly teach that the voltage regulator circuit is a switching voltage regulator. **Hanf et al.** teaches that the voltage regulator circuit is a switching voltage regulator (CL12, L65 to CL13, L15; CL13, L32-48; Figs 6, 7A and 7B), as a switching mode voltage regulator can be activated and deactivated by means of a control signal (CL5, L25-27). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Chen et al.** with the system of **Hanf et al.** that included the voltage regulator circuit being a switching voltage regulator, as a switching mode voltage regulator could be activated and deactivated by means of a control signal.

Response to Amendments

20. Applicants' amendments, filed on February 23, 2004 have been considered. The art rejections are based on the additional prior art included in this office action.

20.1 As per the Applicants' argument that at the time the invention was made, the subject matter of the present application and the primary reference used, **Anderson et al.** (U.S. Patent 6,385,565) was commonly used by Sun Microsystems, Inc. and therefore cannot be used as a 35 USC 103 (a) reference as the current application was filed after November 29, 1999. In response to the Applicants' argument, the Examiner has used new references viz. **Chen et al.** ("On-chip decoupling capacitor optimization for high-performance VLSI design", IEEE, 1998), **Skelton et al.** (U.S. Patent 6,147,478), **Smith** ("Packaging and power distribution design considerations for sun Microsystems desktop workstation", IEEE, 1997) and **O'Sullivan et al.** ("Developing decoupling methodology with SPICE for multilayered printed circuit boards", IEEE, 1998) in this office action.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
August 14, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER